WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

an insulating layer formed on the semiconductor substrate;

a semiconductor layer insulated from the semiconductor substrate by the insulating layer;

source regions of a first conduction type and drain regions of the first conduction type both formed in the semiconductor layer;

body regions of a second conduction type formed in the semiconductor layer between the source regions and the drain regions to store data by accumulating or releasing an electric charge;

word lines formed on the body regions in electrical isolation from the body regions to extend in a first direction;

bit lines connected to the drain regions and extending in a direction different from the first direction; and

buried wirings formed in the insulating layer in electrical isolation from the semiconductor substrate and the semiconductor layer, said buried wirings extending in parallel with the bit lines.

2. A semiconductor integrated circuit device according to claim 1, wherein a plurality of said bit lines extend in equal intervals and said buried wirings equal in number as the bit lines, and extend in the same intervals as those of the bit lines.

3. A semiconductor integrated circuit device according to claim 1, wherein the buried wirings extend in a direction across the word lines.

4. A semiconductor integrated circuit device according

to claim 1, wherein the potential of a first word line of said word lines and the potential of a first buried layer of said buried wirings are driven in the same potential direction to release the electric charge from one body region located at an intersection of the first word line and the first buried wiring.

5. A semiconductor integrated circuit device according to claim 1 further comprising:

a memory cell array including a plurality of said body regions located at intersections of the word lines and the bit lines;

a detector circuit located near a first side of the memory cell array to detect data in the body regions of the memory cell array; and

a drive circuit located near the fist side of the memory cell array to drive the buried wirings.

6. A semiconductor integrated circuit device according to claim 2 further comprising:

a memory cell array including a plurality of said body regions located at intersections of the word lines and the bit lines;

a detector circuit located near a first side of the memory cell array to detect data in the body regions of the memory cell array; and

a drive circuit located near the first side of the memory cell array to drive the buried wirings.

7. A semiconductor integrated circuit device according to claim 1 further comprising:

a memory cell array including a plurality of said body regions located at intersections of the word lines and the bit lines;

a detector circuit located near a first side of the memory cell array to detect data in the body regions of the memory

cell array; and

a drive circuit located near a second side of the memory cell array opposite from the first side thereof to drive the buried wirings.

8. A semiconductor integrated circuit device according to claim 2 further comprising:

a memory cell array including a plurality of said body regions located at intersections of the word lines and the bit lines;

a detector circuit located near a first side of the memory cell array to detect data in the body regions of the memory cell array; and

a drive circuit located near a second side of the memory cell array opposite from the first side thereof to drive the buried wirings.

9. A semiconductor integrated circuit device according to claim 7, wherein a plurality of said memory cell arrays are provided in alignment, and a plurality of detector circuits and the drive circuits are provided alternately in spaces between adjacent said memory cells.

10. A semiconductor integrated circuit device according to claim 8, wherein a plurality of said memory cell arrays are provided in alignment, and a plurality of detector circuits and the drive circuits are provided alternately in spaces between adjacent said memory cells.

11. A semiconductor integrated circuit device according to claim 1, wherein each said buried layer is associated with a plurality of said bit lines.

12. A semiconductor integrated circuit device according to claim 2, wherein each said buried layer is associated with a plurality of said bit lines.

13. A semiconductor integrated circuit device according to claim 1, wherein each said body region constitutes a part of a full depression type memory cell.